AF/2800

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#17 Appeal Brief 4/17/03

Applicant: Michael R. May **Examiner:** Luu, An T
Serial No: 09/626,574 **Art Group:** 2816
Filing Date: 7/27/00 **Docket No:** SIG000049
Title: EDGE SENSITIVE DETECTION CIRCUIT

Date: 3/25/03

Honorable Commissioner of
Patents and Trademarks,
Washington, D.C. 20231

APPELLANT'S BRIEF PURSUANT TO 37 CFR § 1.192

In accordance with a Notice of Appeal filed on 3/24/03, the applicant submits this appellant's brief.

1. The small entity fee for filing a brief in support of an appeal of $160 is hereby authorized to be charged to the Assignee's deposit account 50-1415.

2. Real Party in Interest: All rights to the above referenced patent application have been assigned to:

SigmaTel, Inc.
3815 S. Cap. of Tx. Hwy
Austin, Texas 78704

3. Related Appeals and Interferences: There are no known other appeals or interferences that would directly or indirectly affect the Board's decision in the present appeal.

4. Status of the Claims: The present patent application includes 18 pending claims.

Claims 1, 6, 9, 11, and 15 stand rejected under 35 USC § 102(b) as being anticipated by Farrell et al. (U.S. Patent No. 5,510,740).

Claims 2, 3, and 12 stand rejected under 35 USC § 103(a) as being unpatentable over Farrell in view of Tsukikawa (U.S. Patent No. 6,121,812).

Claims 4, 5, 13, 14, 17, and 18 stand rejected under 35 USC § 103(a) as being unpatentable over Farrell in view of Okada (U.S. Patent No. 4,306,198).

Claims 7, 8, 10, and 16 have been objected to for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. <u>Statement of Amendments</u>: A final office action was mailed for the present patent application on 1/28/03. No response to this office action has been filed.

6. <u>Summary of the Invention</u>: The present invention provides an edge sensitive detection circuit that overcomes the difficulties faced by an integrated system when processing events, such as power down, reset, standby, set, and power up, where the event is triggered via a logic state change. The difficulty arises because the software that overwrites the logic state of the event needs to be active, such that the detection circuit may detect a change in the logic state of the event. However, the processor and memory interfaces cannot be activated to process the software to change the logic state of the event until the detection circuit detects a change in the logic state.

Generally, an edge sensitive detection circuit in accordance with the prevent invention includes a filter module and a soft latch module. The filter module is operably coupled to receive an input logic signal that corresponds to the triggering of an event and produces a pulse signal in response to an edge of the input logic signal. The filter may include a capacitor operably coupled to a controlled impedance, an inverter and a driver transistor, wherein the capacitor senses an edge of the input logic signal and, in combination with the controlled impedance, produces the pulse signal. The soft latch module is operably coupled to receive the pulse signal and to latch a logic value in accordance with the pulse signal.

7. Issues: (1) The applicant contends that the Examiner misapplied the MPEP to substantiate the 35 USC § 102(b) rejection; (2) The applicant contends that claims 1, 6, 9, 11, and 15 are not anticipated by Farrell et al.; (3) The applicant contends that claims 2, 3, and 12 are not rendered obvious by Farrell in view of Tsukikawa. (4) The applicant contends that claims 4, 5, 13, 14, 17, and 18 are not rendered obvious by Farrell in view of Okada.

8. Grouping of the Claims:

Claims 1, 6, 9, 11, and 15 may be grouped for arguments with respect to the 35 USC § 102(b) rejection.

Claims 2, 3, and 12 may be grouped for arguments with respect to the 35 USC § 103(a) rejection as being unpatentable over Farrell in view of Tsukikawa.

Claims 4, 5, 13, 14, 17, and 18 may be grouped for arguments with respect to the 35 USC § 103(a) rejection as being unpatentable over Farrell in view of Okada.

No arguments are being presented for claims 7, 8, 10, and 16.

9. Argument:

A. Claims 1, 6, 9, 11, and 15 have been rejected under 35 USC § 102(b) as being anticipated by Farrell et al.

The Examiner has stated, in an office action mailed 5/3/01, that Farrell discloses in Figure 8 an apparatus comprising a filter 820 received an input signal (reset signal) 802 via a processing element 816 for producing a pulse signal 826 and a latch 824 coupled to the filter for latching the pulse signal as claimed.

This same rejection was reasserted in a final office action mailed on 9/12/01, a subsequent office action mailed on 8/1/02, and again in the present final office action mailed on 1/28/03.

The applicant has argued and maintains the argument of the responses filed on 8/21/01, 3/4/02, and 12/2/02. The argument is as follows:

> Claim 1 of the present invention provides an edge sensitive detection circuit that accurately produces a latched logic value for an integrated circuit when that integrated circuit is in a state of transition (e.g., power down, reset, standby, and/or power up). As claimed, the edge sensitive detection circuit includes a filter module and a soft latch module. The

filter module produces a pulse signal in response to an edge of an input logic signal and provides the pulse signal to the soft latch module. The soft latch module latches a logic value in accordance with the pulse signal.

Because the edge sensitive detection circuit of claim 1 does not require a clock signal to latch a logic signal, the software-hardware interdependency is overcome. As stated in the background section of the present patent application, the software-hardware interdependency results in one portion (e.g., software or hardware) needing the other to be functional before it can be functional in traditional triggering circuits.

The clock synchronizing reset system 112, and its components (i.e., reset conditioning circuitry 804, reset leading edge detector 808, and clock divider 812), of Figure 8 of Farrell are a traditional triggering circuit and hence use a clock signal 102. As taught, a reset signal is applied at least ten times to the input of the clock synchronizing reset system 112 (Column 21, lines 23 - 26). The edge sensitive detection circuit of claim 1 has no such ten-time limitation nor does it include a requirement for a clock signal.

The reset conditioning circuitry 804, which includes synchronizer 816 and reset filter 820, receives the reset signal and produces, based on a clock signal 102, a conditioned reset signal therefrom. The conditioned reset signal must have a predetermined time duration before it is applied to the leading edge detector 808 (Column 21, lines 39 - 44). The edge sensitive detection circuit of claim 1 has no such time duration limitation between generating the pulse by the filter and providing the pulse to the soft latch module.

The leading edge detector 808 of Farrell includes a latch 824 that is clocked by clock input line 102, which supports an externally available clock signal (Column 21, lines 45 - 48). The clock input line 102 also clocks reset conditioning circuitry 804 (Column 21, lines 50 - 51). The edge sensitive detection circuit of claim 1 has no such clocking limitation.

The output of latch 824 is inverted and applied to gate 828, which also receives the conditioned reset signal of line 826. The output of gate 828 is thus representative of the leading edge of the reset signal of input line 802 and it is the output of the reset leading edge detector 808 (column 21, lines 51 - 56). The edge sensitive detection circuit of claim 1 includes no limitation regarding feed-forwarding of a conditioned reset signal to produce a leading edge of that signal.

As such, since the edge sensitive detection circuit of claim 1 does not include limitations with respect to: multiple inputting of a logic signal; time duration of a conditioned input signal; clocking of elements within the circuit; and feed-forwarding of the input signal, claim 1 is not anticipated by Farrell.

In the office action of 8/1/02, in response to the applicant's arguments, the Examiner stated," As to teaching away from claim 1, the recitation of claim recites the transition term "comprises" which is interpreted as "being inclusive or open-ended and does not exclude additional, un-recited elements or method steps" (MPEP Sec. 2111.03). Further, there is no mention of clock input 102 in the rejection of claim. Therefore, the existence of clock input 102 is a non-issue."

The applicant believes that the Examiner has misapplied Section 2111.03 of the MPEP to add limitations to the present claims, which were purposefully excluded from the claims, to substantiate the anticipation rejection in light of Farrell. In *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 227 USPQ 657 (Fed. Cir. 1985), the court clearly looked to what was defined by the claim and interpreted it in the light of the disclosure

upon which the claim was based. The court did not expand the meaning of comprises to include further limitations required by the reference.

In this instance, the claims do not include a clock signal, nor is one described in the specification. In fact, as mentioned above, the detection circuit of the present invention does not require a clock signal to latch a logic signal, which eliminates the software-hardware interdependency. The Farrell reference clearly requires a clock signal for the clock synchronizing reset system 112 to function. Thus, the claims cannot be expanded to include the limitation of a clock signal as is taught and required by Farrell.

Therefore, since the present claimed invention does not include a clock signal limitation as is required by the Farrell reference, Farrell cannot anticipate the present claims. The above-mentioned differences (e.g., multiple inputting of a logic signal; time duration of a conditioned input signal; and feed-forwarding of the input signal) further distinguish the present claims from Farrell.

B. Claims 2, 3, and 12 have been rejected under 35 USC § 103(a) as being unpatentable over Farrell in view of Tsukikawa.

The applicant reasserts the arguments presented in the preceding section with respect to Farrell. Since Farrell does not teach or suggest an edge sensitive detection circuit as is presently claimed in claims 1 and 9, the dependent claims 2, 3, and 12 cannot be rendered obvious by

Farrell in view of Tsukikawa. In addition, the latch shown in figure 8 of Tsukikawa includes three logic elements NOR gate 41, inverter 42, and AND gate 43 and does not include an impedance. In contrast, the soft latch of the present claims includes two logic elements and an output impedance associated with the second logic element.

C. Claims 4, 5, 13, 14, 17, and 18 have been rejected under 35 USC § 103(a) as being unpatentable over Farrell in view of Okada.

The applicant reasserts the arguments presented above with respect to Farrell. Since Farrell does not teach or suggest an edge sensitive detection circuit as is presently claimed in claims 1, 9, and 17 the dependent claims 4 and 5 of claim 1, dependent claims 13 and 14 of claim 9, and dependent claim 18 of claim 17 cannot be rendered obvious by Farrell in view of Okada. In addition, the filter shown in figure 3 of Okada is substantially different than the filter module of the present invention. In particular, the filter of Okada includes a differential amplifier (Q2 and Q3) and a bias voltage source V_{BB}, and does not include an inverter. The filter of the present claims includes an inverter and does not include a differential amplifier or a bias voltage source.

RESPECTFULLY SUBMITTED,

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CERTIFICATE OF MAILING

37 C.F.R 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231, on the date below:

3/31/03 — Date

Diane Hudson — Signature

Copy of Claims

1. An edge sensitive detection circuit comprising:

a filter module operably coupled to receive an input logic signal, wherein the filter module produces a pulse signal in response to an edge of the input logic signal; and

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

2. (amended) The edge sensitive detection circuit of claim 1, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.

3. (amended) The edge sensitive detection circuit of claim 2, wherein the second inverting logic element comprises an inverter and wherein the first inverting logic element comprises at least one of an inverter and a NAND gate.

4. The edge sensitive detection circuit of claim 1, wherein the filter module comprises:

a capacitor operably coupled to receive the input logic signal; and

a gating circuit operably coupled to the capacitor, wherein the gating circuit generates the pulse signal, wherein the capacitor and an impedance of at least one element of the gating circuit are tuned based on at least one of rise time or fall time of the input logic signal.

5. The edge sensitive detection circuit of claim 4, wherein the gating circuit comprises:

an inverter, wherein an output of the inverter is operably coupled to a drive transistor; and

a controlled impedance coupled to the capacitor, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor.

6. The edge sensitive detection circuit of claim 1, wherein the input logic signal is at least one of: a reset signal, a power down signal, a power up signal, a standby signal, and a set signal.

7. The edge sensitive detection circuit of claim 1 further comprises a second filter module operably coupled to receive a second input logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second input logic signal, and wherein the

soft latch module latches the logic value in accordance with the second pulse signal.

8. The edge sensitive detection circuit of claim 7, wherein the second filter module comprises:

a second capacitor operably coupled to receive the second input logic signal; and

a second gating circuit operably coupled to the second capacitor, wherein the gating circuit generates the second pulse signal, wherein the second capacitor and an impedance of at least one element of the second gating circuit are tuned based on at least one of rise time or fall time of the second input logic signal.

9. A edge sensitive detection circuit comprises:

an input gating device;

a processing module operably coupled to the input gating device, wherein the processing module utilizing operational instructions to process an input logic signal from the input gating device to produce a processed logic signal;

a filter module operably coupled to receive the processed logic signal, wherein the filter module produces a pulse signal in response to an edge of the processed logic signal; and

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

10. (amended) The edge sensitive detection circuit of claim 9 further comprises:

a second gating device that provides a second input logic signal to the processing module, wherein the processing module produces a second processed logic signal based on the second input logic signal;

a second filter module operably coupled to receive the second processed logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second processed logic signal; and

a second soft latch module operably coupled to receive the second pulse signal, wherein the second soft latch module latches a logic value in accordance with the second pulse signal.

11. The edge sensitive detection circuit of claim 9, wherein the input gating device provides one of a plurality of input logic signals as the input logic signal.

12. (amended) The edge sensitive detection circuit of claim 9, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.

13. The edge sensitive detection circuit of claim 9, wherein the filter module comprises:

a capacitor operably coupled to receive the input logic signal; and

a gating circuit operably coupled to the capacitor, wherein the gating circuit generates the pulse signal, wherein the capacitor and an impedance of at least one element of the

gating circuit are tuned based on at least one of rise time or fall time of the input logic signal.

14. The edge sensitive detection circuit of claim 13, wherein the gating circuit comprises

an inverter, wherein an output of the inverter is operably coupled to a drive transistor; and

a controlled impedance coupled to the capacitor, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor.

15. The edge sensitive detection circuit of claim 9, wherein the input logic signal comprises at least one of: a reset signal, a set signal, a power down signal, a power on signal, and a standby signal.

16. The edge sensitive detection circuit of claim 9 further comprises a second filter module operably coupled to receive a second input logic signal, wherein the second filter module produces a second pulse signal in response to an edge of the second input logic signal, and wherein the soft latch module latches the logic value in accordance with the second pulse signal.

17. An edge sensitive detection circuit comprising:

a capacitor operably coupled to receive the input logic signal;

a controlled impedance coupled to the capacitor, wherein the capacitor and an impedance of at least one element of a gating circuit are tuned based on at least one of rise time or fall time of the input logic signal;

an inverter, wherein an input of the inverter is operably coupled to the coupling of the controlled impedance to the capacitor;

a drive transistor operably coupled to produce a pulse signal, wherein an output of the inverter is operably coupled to the drive transistor;

a soft latch module operably coupled to receive the pulse signal, wherein the soft latch module latches a logic value in accordance with the pulse signal.

18. (amended) The edge sensitive detection circuit of claim 17, wherein the soft latch module comprises:

a first inverting logic element; and

a second inverting logic element having an output impedance, wherein an input of the first inverting logic element is coupled to the output impedance, wherein an input of the second inverting logic element is coupled to

an output of the first inverting logic element, and wherein the pulse signal is received at the coupling of the input of the first inverting logic element and the output impedance.